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ABSTRACT OF THE DISCLOSURE

An ESD protection structure for use with ICs that can protect from ESD events of both positive and negative polarities, has a low snapback holding voltage and a high maximum snapback current. The ESD protection structure includes a semiconductor substrate of a first conductivity type (typically P-type), and first and second well regions of a second conductivity type (typically N-type) disposed in the substrate. The first and second well regions are separated by a gap region of the first conductivity type in the substrate. Also included are first and second floating regions (of the second conductivity type) disposed in the first and second well regions adjacent to the gap region, respectively. The ESD protection structure also includes first and second contact regions of the first conductivity type disposed on the first and second well regions, respectively, and spaced apart from the first and second floating regions, respectively. The ESD protection structure further includes first and second contact regions of the second conductivity type disposed on the first and second well regions, respectively, and spaced apart from the first and second floating regions, respectively. During operation, the ESD protection structure undergoes primary breakdown by low current avalanche breakdown of the gap region between the first and second floating regions, followed by "double injection" of both holes and electrons, thereby providing for a low snapback holding voltage and a high maximum snapback current. The symmetrical nature of the ESD protection structure provides for protection from both positive and negative ESD events.